CLAIMS:

1. A PLL circuit comprising:

a phase comparator with current mode output;

a low-pass filter; and

a VCO,

wherein in the case where a convergence frequency of the PLL circuit is lower than a setting frequency, the PLL circuit converges the convergence frequency by a PLL feedback loop within a range from an input voltage lower than a convergence voltage corresponding to the convergence frequency to the convergence voltage, and

wherein in the case where the convergence frequency of the PLL circuit is higher than the setting frequency, the PLL circuit converges the convergence frequency by the PLL feedback loop within a range from an input voltage higher than a convergence voltage to the convergence voltage.

2. A PLL circuit comprising:

a phase comparator with current mode output;

a low-pass filter; and

a VCO,

wherein in the case where a convergence frequency of the PLL circuit is higher than a setting frequency, the PLL circuit converges the convergence frequency by a PLL feedback loop within a range from an input voltage higher than a convergence voltage corresponding to the convergence frequency to the convergence voltage; and

wherein in the case where the convergence frequency of the PLL circuit is lower than the setting frequency, the PLL

circuit converges the convergence frequency by a PLL feedback loop within a range from an input voltage lower than a convergence voltage to the convergence voltage.

3. A PLL circuit comprising:

a phase comparator with current mode output, for outputting a signal proportional to a phase difference between first input signal modulated in its frequency and second input signal;

a low-pass filter connected to an output terminal of the phase comparator with current mode output;

a VCO connected to an output terminal of the low-pass filter;

a mixer connected to an output terminal of the VCO and converting an output frequency of the VCO so as to output a second signal;

first to third constant current sources connected to the output terminal of the phase comparator with current mode output;

a switch connected between the phase comparator with current mode output and a reference voltage; and

control means for controlling an on-off of the first to third constant current sources and controlling a short-circuit and open of the switch.

4. The PLL circuit according to claim 3,

wherein the reference voltage is 0V,

wherein the first and third constant current sources output a constant current to the output terminal of the phase

comparator with current mode output, and

wherein the second constant current source inputs a constant current from the output terminal of the phase comparator with current mode output.

5. The PLL circuit according to claim 3,

wherein the reference voltage is a power-supply voltage,

wherein the first and third constant current sources input a constant current from the output terminal of the phase comparator with current mode output, and

wherein the second constant current source outputs a constant current to the output terminal of the phase comparator with current mode output.

6. The PLL circuit according to claim 4,

wherein the PLL circuit is constructed in a manner that in a non-operating state, the first to third constant current sources are in an off state so that the switch is short-circuited, and first and second means are used for a transfer from the non-operating state to an operating state, and further, the first means is used in the case where a convergence frequency of the PLL circuit satisfies a condition that it is a frequency between an output frequency of the VCO in short-circuit of the switch and a setting frequency, while the second means is used in the case where it does not satisfy the condition,

wherein the first means opens the switch and turns on the first constant current source, and

wherein the second means opens the switch and turns on

the third constant current source, and turns off the third constant current source while turning on the second constant current source, after a predetermined time elapses.

7. The PLL circuit according to claim 5,

wherein the PLL circuit is constructed in a manner that in a non-operating state, the first to third constant current sources are in an off state so that the switch is short-circuited, and first and second means are used for a transfer from the non-operating state to an operating state, and further, the first means is used in the case where a convergence frequency of the PLL circuit satisfies a condition that it is a frequency between an output frequency of the VCO in short-circuit of the switch and a setting frequency, while the second means is used in the case where it does not satisfy the condition,

wherein the first means opens the switch and turns on the first constant current source, and

wherein the second means opens the switch and turns on the third constant current source, and turns off the third constant current source while turning on the second constant current source, after a predetermined time elapses.

8. The PLL circuit according to claim 6,

wherein output current values of the first and second constant current sources are equal to each other, and an output current value of the second constant current source is at least twice or more as much as the output current values of the first and third constant current sources.

9. The PLL circuit according to claim 7,

wherein output current values of the first and second constant current sources are equal to each other, and an output current value of the second constant current source is at least twice or more as much as the output current values of the first and third constant current sources.

10. A PLL circuit comprising:

a phase comparator with current mode output, for outputting a signal proportional to a phase difference between first input signal modulated in its frequency and second input signal;

a low-pass filter connected to an output terminal of the phase comparator with current mode output;

a VCO connected to an output terminal of the low-pass filter;

a mixer connected to an output terminal of the VCO and converting an output frequency of the VCO so as to output a second signal;

first and second constant current sources connected to the output terminal of the phase comparator with current mode output;

a first switch connected between the phase comparator with current mode output and a first reference voltage;

a second switch connected between the phase comparator with current mode output and a second reference voltage; and

control means for controlling an on-off of the first and second constant current sources and controlling a short-circuit

and open of the first and second switches.

11. The PLL circuit according to claim 10,

wherein the first reference voltage is 0V,

wherein the second reference voltage is a power-supply voltage,

wherein the first constant current sources outputs a constant current to the output terminal of the phase comparator with current mode output, and

wherein the second constant current source inputs a constant current from the output terminal of the phase comparator with current mode output.

12. The PLL circuit according to claim 10,

wherein the first reference voltage is a power-supply voltage,

wherein the second reference voltage is 0V,

wherein the first constant current sources inputs a constant current from the output terminal of the phase comparator with current mode output, and

the second constant current source outputs a constant current to the output terminal of the phase comparator with current mode output.

13. The PLL circuit according to claim 11,

wherein the PLL circuit is constructed in a manner that in a non-operating state, the first and second constant current sources is in an off state so that the first switch is short-circuited and so that the second switch is opened, and first and second means are used for a transfer from the non-operating

state to an operating state, and further, the first means is used in the case where a convergence frequency of the PLL circuit satisfies a condition that it is a frequency between an output frequency of the VCO in short-circuit of the first switch and a setting frequency, while the second means is used in the case where it does not satisfy the condition,

wherein the first means opens the first switch and turns on the first constant current source, and

wherein the second means opens the first switch and short-circuits the second switch, and opens the second switch while turning on the second constant current source, after a predetermined time elapses.

14. The PLL circuit according to claim 12,

wherein the PLL circuit is constructed in a manner that in a non-operating state, the first and second constant current sources is in an off state so that the first switch is short-circuited and so that the second switch is opened, and first and second means are used for a transfer from the non-operating state to an operating state, and further, the first means is used in the case where a convergence frequency of the PLL circuit satisfies a condition that it is a frequency between an output frequency of the VCO in short-circuit of the first switch and a setting frequency, while the second means is used in the case where it does not satisfy the condition,

wherein the first means opens the first switch and turns on the first constant current source, and

wherein the second means opens the first switch and

short-circuits the second switch, and opens the second switch while turning on the second constant current source, after a predetermined time elapses.

15. The PLL circuit according to claim 13,

wherein output current values of the first and second constant current sources are equal to each other.

16. The PLL circuit according to claim 14,

wherein output current values of the first and second constant current sources are equal to each other.

17. A PLL circuit comprising:

a phase comparator with current mode output, for outputting a signal proportional to a phase difference between first input signal modulated in its frequency and second input signal;

a low-pass filter connected to an output terminal of the phase comparator with current mode output;

a VCO connected to an output terminal of the low-pass filter;

a mixer connected to an output terminal of the VCO and converting an output frequency of the VCO so as to output a second signal;

a variable current source and a constant current source connected to the output terminal of the phase comparator with current mode output;

a switch connected between the phase comparator with current mode output and a first reference voltage; and

control means for controlling an on-off of the variable

current source, an output current value, an on-off of the constant current source, and controlling a short-circuit and open of the switch.

18. The PLL circuit according to claim 17,

wherein the reference voltage is 0V,

wherein the variable current source outputs a current to the output terminal of the phase comparator with current mode output, and

wherein the constant current source inputs a constant current from the output terminal of the phase comparator with current mode output.

19. The PLL circuit according to claim 17,

wherein the reference voltage is a power-supply voltage,

wherein the variable current source inputs a current from the output terminal of the phase comparator with current mode output, and

wherein the constant current source outputs a constant current to the output terminal of the phase comparator with current mode output.

20. The PLL circuit according to claim 18,

wherein the PLL circuit is constructed in a manner that in a non-operating state, the variable current source and the constant current sources are in an off state, the switch is short-circuited, and first and second means are used for a transfer from the non-operating state to an operating state, and further, the first means is used in the case where a convergence frequency of the PLL circuit satisfies a condition

that it is a frequency between an output frequency of the VCO in short-circuit of the first switch and a setting frequency, while the second means is used in the case where it does not satisfy the condition,

wherein the first means opens the switch and turns on the variable current source so that the variable current source outputs a first constant current value, and

wherein the second means opens the switch and turns on the variable current source so that the variable current source outputs a second constant current value, and turns off the variable current source while turning on the constant current source, after a predetermined time elapses.

21. The PLL circuit according to claim 19,

wherein the PLL circuit is constructed in a manner that in a non-operating state, the variable current source and the constant current sources are in an off state, the switch is short-circuited, and first and second means are used for a transfer from the non-operating state to an operating state, and further, the first means is used in the case where a convergence frequency of the PLL circuit satisfies a condition that it is a frequency between an output frequency of the VCO in short-circuit of the first switch and a setting frequency, while the second means is used in the case where it does not satisfy the condition;

wherein the first means opens the switch and turns on the variable current source so that the variable current source outputs a first constant current value, and

wherein the second means opens the switch and turns on the variable current source so that the variable current source outputs a second constant current value, and turns off the variable current source while turning on the constant current source, after a predetermined time elapses.

22. The PLL circuit according to claim 20,

wherein the first constant current value and an output current value of the constant current are equal to each other, and the second constant current value is at least twice or more as much as the first constant current value and the output current value of the current value.

23. The PLL circuit according to claim 21,

wherein the first constant current value and an output current value of the constant current are equal to each other, and the second constant current value is at least twice or more as much as the first constant current value and the output current value of the current value.

24. A wireless mobile station comprising:

a base band circuit;

a modulator for inputting a first base band signal from the base band circuit;

a PLL circuit connected to an output of the modulator;

a power amplifier connected to an output of the PLL circuit;

a receiver circuit for outputting a second base band signal to the base band circuit;

an antenna; and

a selector connected with the antenna, an input of the receiver circuit and an output of the power amplifier;

wherein the base band circuit outputs a control signal for controlling an operation of the wireless mobile station; and

wherein the PLL circuit comprises:

a phase comparator with current mode output, for outputting a signal proportional to a phase difference between first input signal modulated in its frequency and second input signal;

a low-pass filter connected to an output terminal of the phase comparator with current mode output;

a VCO connected to an output terminal of the low-pass filter;

a mixer connected to an output terminal of the VCO and converting an output frequency of the VCO so as to output a second signal;

first and second constant current sources connected to the output terminal of the phase comparator with current mode output;

a first switch connected between the phase comparator with current mode output and a first reference voltage;

a second switch connected between the phase comparator with current mode output and a second reference voltage; and

control means for controlling an on-off of the first and second constant current sources and controlling a short-circuit and open of the first and second switches.

25. A wireless mobile station comprising:

a base band circuit;

a modulator for inputting a first base band signal from the base band circuit;

a PLL circuit connected to an output of the modulator;

a power amplifier connected to an output of the PLL circuit;

a receiver circuit for outputting a second base band signal to the base band circuit;

an antenna; and

a selector connected with the antenna, an input of the receiver circuit and an output of the power amplifier,

wherein the base band circuit outputs a control signal for controlling an operation of the wireless mobile station, and

wherein the PLL circuit comprises:

a phase comparator with current mode output;

a low-pass filter; and

a VCO,

wherein in the case where a convergence frequency of the PLL circuit is lower than a setting frequency, the PLL circuit converges the convergence frequency by a PLL feedback loop within a range from an input voltage lower than a convergence voltage corresponding to the convergence frequency to the convergence voltage, and

wherein in the case where the convergence frequency of the PLL circuit is higher than the setting frequency, the PLL

circuit converges the convergence frequency by the PLL feedback loop within a range from an input voltage higher than a convergence voltage to the convergence voltage.